GEDIZ ÜNİVEBSİTESİ	Engineering and Architecture Faculty	Course Information
izmir	Computer Engineering Department	Form

COURSE INFORMATION

Academic Year / Semester		2011 – 2012 / Fall
Course Code, Name, Credits (T-A-C)		EEE 251 Logic Design and Circuits (3-2-4)
Lecture and Lab	Theoretical	Tuesday, 10:00 – 12:45
Schedules	Lab	Tuesday, 13:45 – 15:30
Course Type		Compulsory
Prerequisite		None

ACADEMIC PERSONAL

Title / First and Last Name	Prof. Dr. Haluk Gümüşkaya	
Room	D107	
E-Mail Address / Web Page	haluk@gumuskaya.com http://www.gumuskaya.com	
Telephone	0232-355 0000 - 2305	
Office Hours Tuesday: 09:00 – 10:00, Wednesday: 09:00 – 10:00		
Assistant	Yavuz İnce	

COURSE DESCRIPTION

Data representation, number systems, arithmetic operations, Boolean algebra, logic functions and theorems, logic gates, canonical forms, simplification techniques, design of combinational circuits, decoders, encoders, multiplexers, arithmetic circuits, sequential circuits, design of sequential circuits and the algorithmic state machine, timing and timing problems, programmable logic devices, registers and register operations, buses and 3-state logic, basics of memory, SRAM and DRAM, introduction to basic computer organization and design.

COURSE TEXTBOOK AND OTHER MATERIALS

Main Book	1. Digital Design with RTL Design, Verilog and VHDL, 2nd ed., Frank Vahid, John Wiley, 2011.	
Lab Resources	1. Hardware equipment provided in the Digital Systems Design Lab.	
	2. VHDL tools	
	3. NI Circuit Design Suit 11.0 – Multisim	
Recommended	1. Logic and Computer Design Fundamentals, 4th Ed., M. Morris Mano, C. Kime, Prentice Hall, 2008.	
Books	2. Digital Design, 4th Ed., M. Morris Mano, M. D. Ciletti, Prentice Hall, 2007.	

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WEEKLY COURSE SCHEDULE

W	D	Topics Covered	
1	27/09	Introduction, digital and binary data representation, DD Chp. 1	
2	4/10	Switches, transistors, logic gates, Boolean algebra, DD Chp. 2.1-2.5	
3	11/10	Truth tables, canonical forms, combinational design process, examples, DD Chp. 2.6-2.8	
4	18/10	Decoders and MUXes, non-ideal behavior, Verilog modeling, DD Chp. 2.9, 2.10	
5	25/10	Latches & flip-flops, basic register, clocking, FSMs, DD Chp. 3.1-3.3	
6	1/11	Controller design, examples, non-ideal behavior, Verilog modeling, DD Chp. 3.4, 3.5, 3.8	
7	8/11	No classes, Kurban Bayram week	
8	15/11	Registers, adders, comparator, multiplier, Midterm exam (Nov 15), DD Chp. 4.1-4.5	
9	22/11	Signed numbers, subtractors, ALUs, shifters, counters, timers, register file, Verilog modeling, DD Chp. 4.6-4.10, 4.13	
10	29/11	High-level state machines HLSM, RTL design process, examples, DD Chp. 5.1-5.3	
11	6/12	RTL design (continued), clock frequency, behavioral design, memory, RAM, ROM, DD DD Chp. 5.4- 5.7	
12	13/12	Queues/FIFO, multiple processors, heirarchy, Verilog modeling, DD Chp. 5.6-5.10, 5.13	
13	20/12	Optimizations and tradeoffs, DD Chp. 6	
14	27/12	Physical implementation on ICs, DD Chp. 7	
15	3/01	Reserved	

WEEKLY LABORATORY SCHEDULE

Week	Date	Subjects
1		
2		
3		
4		ТВА
5		ТВА
6		ТВА
7		No classes, Kurban Baytam week
8		No lab

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9	ТВА
10	ТВА
11	ТВА
12	ТВА
13	ТВА
14	ТВА
15	ТВА

	If Applicable Put (X) Sign	Percent (%)
Midterm I	X	20
Midterm II		
Quizzes		
Homework		20
Laboratory	X	30
Term Project	X	
Other (Attendance,)		
Final Exam	Х	30

In order to pass EEE 251, students must show minimum competence in the exams. Any student who does not have a weighted average of 35.0 or greater for midterm and final exams will receive an automatic grade of FF, for lack of minimum competence. The weighted average will be calculated as follows: $(0.20 \times Midterm Exam + 0.30 \times Final Exam) / 0.50$

Attendance: Students who fail to attend at least 70% of the classes will receive a grade of FF. Students must not miss more than 2 lab sessions (80% of the lab sessions), or they will receive a grade of FF.

Students who meet the above requirements will have their numerical course average calculated with the following weights:

Labs:30%Homework:20%Midterm Exam:20%Final Exam:30%

From the numerical course average grades, the students who meet the above two requirements, letter grades ranging from AA to FF will be determined in the usual way (taking into account overall performance and distribution of the scores, class and lab participation and effort, as well as the attendance (in class and lab) of the student.